IN THE SPECIFICATION

Please amend the specification as follows:

The paragraph beginning at page 4, line 16, is amended as follows:

When logic output node 110 above the N-stack is pulled down to a low voltage by the N-stack, and then the path through the N-stack goes to a high impedance, the combination of P-channel transistors 102 and 104 and inverters 112 and 116 [[114]] automatically cause the voltage on logic output node 110 to reset to a high voltage. Inverter 112 drives P-channel transistor 104 off, and inverter 116 drives P-channel transistor 102 on, which pulls up logic output node 110 to a high voltage. After logic output node 110 transitions to a high voltage, inverter 112 drives P-channel transistor 104 [[114]] on, and the circuit reaches steady state with logic output node 110 at a high voltage. The "self-resetting" action just described gives rise to the name "self-resetting circuit." The path through the inverter chain to P-channel transistor 102 and back to logic output 110 is termed the "self-reset path." After output node 110 is reset to [[to]] a high voltage, inverter 112 and P-channel transistor 104 act to maintain or "keep" the output high until some later time when the N-stack inputs cause node 110 to go low. This is termed the "keeper path."